Development of an innovative sequencer and data acquisition (SDAQ) electronics based on FPGA for a CCD timing and signal processing

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ABSTRACT

We report on the performance and characteristics of the SDAQ electronics board developed at the XUVLab of the Department of Physics and Astronomy, University of Florence, as a digital system to control signal generation and data acquisition, mainly designed for new generation CCD cameras, but suitable for driving and acquiring data from a large variety of solid state detector electronics.
This report describes the characteristics of the SDAQ controller as well as the tests and the characterization procedures at XUVLab electronics facilities.

Keywords: programmable logics, FPGAs, microcontrollers, CCD cameras, solid state detectors
1. INTRODUCTION

There are a lot of application areas of CCDs in ground and space based astrophysics and earth observation, which could benefit from compact and versatile control electronics. These include imaging and spectroscopy from UV to IR, auto-guiding, star tracking and wavefront sensors for adaptive optics. In particular, the high level of versatility and programmability, allows for fast and reliable setting of CCD phases generation and data acquisition for several CCD types and formats. Moreover, the high level of integration is suitable for smaller controllers and reduced power consumptions and mass that permits their use in a large area of research fields, mainly for laboratory purposes and ground-based astronomy but, with some modifications for redundancies and space-reliability, also for space-based astrophysics, by means of sub-orbital rockets and satellites hosting imaging cameras.

Here, we describe a Sequencer and Data Acquisition (SDAQ) board we developed for integrating the complete functionality of a dedicated programmable waveform generator with data acquisition capabilities, to provide both a CCD controller and a data acquisition system on a single board. The board can implement waveform resolutions at a clock rate up to 100 MHz, implementing generation of control signals and fast data acquisition procedures.

It is designed specifically to provide programmable detector waveform generation and data acquisition procedures, providing low circuit complexity, PCB circuit size, and power dissipation compared to older DSP or general-purpose microprocessor-based design solutions. Thus, more compact and lightweight cameras can be produced keeping the capability of programming any CCD waveform patterns, such as windowing and/or pixel binning and data acquisition algorithms. A second generation SDAQ design could be simply produced on a radiation hard device implementing redundant logic structures in a structured hardware description language paradigm, for applications in sub-orbital or space experiments requiring CCD cameras.

The SDAQ electronics was originally designed and developed as a core controller for a new CCD camera for the CAOS spectrograph at the Catania Astrophysical Observatory [1], but it is can be used as timing and control signal generator and data acquisition system for other kinds of sensors as diamond-based array detectors.

2. THE SEQUENCER AND DATA ACQUISITION (SDAQ) ELECTRONICS

The SDAQ board is logically structured in three sections:

- SEQUENCER, for detector timing and signal generation;
- DATA ACQUISITION, to acquire digital data from an external 16-bit resolution analog to digital converter (ADC);
- INTERFACE, for communications with a PC or a laptop interfacing the board.
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The SDAQ circuit is designed to manage the clock timing required by any pixelated detector (mainly a CCD sensor), the data acquisition procedures and I/F functions. Fig. 1 shows a schematic diagram representing the SDAQ architecture. The dual function of this circuit is clearly shown in this diagram [2].

In order to accomplish such functions, we selected programmable components, as an FPGA (Field Programmable Gate Array) and a microcontroller (µC), supported by on-board PROM (not shown in Fig. 1, but visible in Fig. 2) and six banks of RAM memories (6x16 Mbit Static RAM) and interfaced through Ethernet 10/100 Mbps or USB modules. While FPGA handles high frequency signals and data addressing and processing, the µC performs the high-level operations (communication I/F, commands management).

![Figure 1. Schematic diagram of the SDAQ architecture.](image)

The communication I/F is one of the tasks of the µC that is accomplished through the USB and Ethernet ports by means of an external integrated module (XPORT module).

The DAQ system consists basically of a 12-MB SRAM controlled by the FPGA; this stores the 16-bits ADC data and waits for the request signal to send them to the µC. Then, the µC sends the data to the computer, through the USB port. The FPGA keeps the core program to operate the Sequencer and DAQ; its design meets the required level of versatility. Owing to the widely available resources and the capability of high-frequency operations (100 MHz clock) of this device, it was possible to implement a modular design, a high level of configurability and a high time resolution (10 ns).

Parameter configuration is not useful for CCD camera end users, but it is crucial for tests and optimization; therefore, some parameters are “frozen” after testing sessions (see section 3).
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All the bias voltages necessary to supply the circuits are generated on-board (CMOS +3.3V and TTL +5V levels), requiring only a supply voltage ranging from 18V to 36V as input, thanks to two TRACO POWER DC-DC switching converters. Other useful voltages like +1.2V and +2.5V are generated thanks to common voltage regulators integrated circuits.

The board can be connected to a bus or a backplane board by means of a DIN 96-pin connector that assure an optimal and reliable mechanical and electrical interface.

![Image of SDAQ board](image.png)

Figure 2. The SDAQ board in EuroCard format (160 mm x 100 mm).

All the I/O signals are buffered by means of octal buffer line drivers (74HC244 IC); level shifting, allowing data transfer in a multi-voltage system, is performed through Maxim MAX3002 voltage level translators.

The board can also mount a MAX3250 RS232 transceiver available for double serial lines if debug procedures or serial communication with other electronics systems is required.

2.1. The Sequencer section

The Sequencer is devoted to the generation of digital clocks to readout detectors [3]. It can be considered also as Logic Board or Timing Circuit; its main task is to provide digital clocks to a Clock Driver and other digital signals like the Clamp and Sample signals to a Correlated Double Sampling circuit (CDS) and the Start Convert to drive the A/D conversion from an external board.

Many detectors are available on the market; they differ for number of pixels, size of sensitive area, number of read-out circuits and bias voltages; however, they are basically driven by
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digital signals that are adapted, buffered and converted to the analog domain by means of a Clock Driver board.
Each of these detectors has to be driven properly; thus, it is necessary to define the Sequencer properties and functional philosophy. In particular, our design was developed to obtain high versatility and compactness and, at the same time, to accomplish all the requirements from new generation CCDs, with wide area or with a mosaic conception, using emergent technologies in the field of electronics. So, we decided to develop a timing circuit using a last generation FPGA logic device implementing a structured and versatile VHDL (VHSIC Hardware Description Language, where VHSIC means Very-High-Speed Integrated Circuits) design. Programmable logics, introduced by some manufacturers, make use of FLASH-programming technology. This allows for programming logic components quickly and on board by means of a specific cable (JTAG cable), reducing significantly the device development phase.
The main features of our design are:

- flexibility: the component can be quickly and simply re-programmed by FLASH technology; to accomplish this task we use a 2Mbit PROM memory (Xilinx XCF02S) in boundary scan configuration;
- stable and reliable clocks: once programmed, FPGA acts as a not programmable hardware; therefore, it is unaffected by jitter noise;
- certified timings: programmable logics have maximum propagation delay times specified by the manufacturer. Moreover, after the implementation of a project, mutual delays between all pins can be firstly simulated and then verified and more than one error or warning report is generated.
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Figure 3. A set of E2V-4240 CCD serial register clocks (horizontal phases) generated by the Sequencer and shaped by means of a clock-driver electronics.

All the processes and clock signals (see Fig. 3) are driven by means of asynchronous finite state machines: the top-level one interfaces microcontroller I/O ports thanks to a 4 x 16 decoder. It decodes commands from the high level software GUI (Graphical User Interface) that interfaces the microcontroller firmware written in C language.

Actually, the VHDL project implemented in the FPGA Xilinx Spartan 3 XC3S200 model, that we selected for our design, is able to generate 8 clocks and 3 control signals for a particular CCD sensor and readout electronics, the E2V-4240 detector with frame format 2048 x 2048 pixels, chosen for the CAOS spectrograph at the Catania Astrophysical Observatory. Nevertheless, the SDAQ board is able to generate more phases and control signals, in a structured manner, designed by means of finite state machine algorithms controlling delays, glitch phenomena and buffering the clocks. In fact, the selected FPGA implements 200K system gates, 4320 logic cells and is provided by a large number of LVTTL compatible I/O pins (up to 173 I/O) thanks to its large package (208 pins).

Figure 4. A typical ModelSim simulation session for E2V CCD-4240 horizontal and vertical phases with binning 2 x 2.

All the developing and programming sequences are performed by means of the freeware Xilinx web-pack ISE Design Suite 10.1 in combination with ModelSim XE III (see Fig. 4), an
Development of an innovative sequencer and data acquisition (SDAQ) electronics based on FPGA for a CCD timing and signal processing integrated environment for design development as schematics or VHDL codes, necessary to simulate, route and synthesize projects.

The VHDL project is mainly composed by three sections:

- the control logic functional block managing the operational modes like "test mode" for sequencer and DAQ testing and "setup mode", e.g. for setting acquisition procedures and cleaning detector procedures;
- the phase and exposure time control block, generating control signals, horizontal and vertical phases and managing the exposure time and the shutter trigger;
- the communication interface block, interfacing microcontroller and managing commands from the high level SW interface.

In particular, the phase control block is very flexible because it is based on a parametric phase generation section and on a counter section that numbers phases. So, it is possible to set up the phase duration (on multiples of base time) and the phase duty cycle owing to internal counters, and ultimately to set the number of phase periods. It is also possible to change quickly the base time thanks to an implemented clock divider block setting the reference time as multiple of the physical clock period.

### 2.2. The DAQ section

The DAQ hardware interfaces digital or analog signals to the PC. It could be in the form of modules that can be connected to the computer ports (parallel, serial, USB, etc.) or cards connected to standard slots (PCI, ISA, etc.) into the motherboard.

![Figure 5. Data acquisition and processing flow inside SDAQ board.](image)

Our design implements a stand-alone module that is connected to a USB or Ethernet computer port and is able to send or receive data and commands to and from the high level SW
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interface. The data acquisition and processing flow, from the converter to the PC, is shown in Fig. 5. Firstly, 16 bits/pixel format data are transferred to the FPGA and then to the SRAM memory buffer, before being readout via a microcontroller interfacing FPGA. The DAQ internal logic is mainly composed by three parts:

- an input 2k x 16 bit FIFO (First In First Out) memory and its controller;
- a SRAM external memory controller;
- an output 2k x 16 bit FIFO memory and its controller.

FIFO memories are used as buffer memories between two asynchronous systems. In fact, they interfaces input data from A/D converter (16 bit @ the ‘start convert’ signal frequency) and output data to microcontroller. FIFO memories are implemented inside FPGA by means of the Xilinx CORE Generator, a useful tool for memory logic block generation and control. Their format and data depth can be simply parameterized before synthesize the VHDL project; so, we chose a 2k format for buffering a 2kpx CCD row (2048 px @ 16 bit) at a time.

The FIFOs and SRAM controllers characterize the DAQ core. The latter is capable to address 16-bit data through a bidirectional port by means of a signal for memory enabling and a 20-bit address. We chose this configuration to assure continuous data flow from the A/D converter to the microcontroller output at a rate fixed by the analog to digital conversion signal, generated by Sequencer and ranging the ADC characteristics (start convert signal).

The use of the bidirectional port is switched between SRAM memories and input and output FIFOs. While input FIFO is continuously filled by incoming data, output FIFO is filled and emptied at a 2kpx (4kBytes) data rate packets. In fact, while microcontroller reads data already stored into the output FIFO, data flows directly from AD converter to the SRAM blocks through the input FIFO. When output FIFO is empty, the SRAM controller enables data reading from RAM, disabling data writing operation to RAM from input FIFO. So, the latter acts as a buffer memory, waiting for a new SRAM write cycle.

SRAM controller addresses data serially and manages memories altogether as a large FIFO, exploiting a dual set of SW pointers for reading and writing procedures. Pointers are refreshed by means of two counters that act incrementing addresses for writing or reading the following memory location. In this way SRAM memories are managed by means of asynchronous signals with respect to the 100 MHz main clock; so, high frequency clock is only fed to the FPGA avoiding interference phenomena on the board.
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2.3. The SDAQ firmware

The SDAQ board firmware (FW) includes the microcontroller FW and the FPGA FW (stored in a dedicated PROM at the bootstrap and loaded afterward to the FPGA).

**Microcontroller FW**

The microcontroller FW was developed under C language with CCS (Custom Computer Service Inc.) compiler, to compile C files and related header files to Assembler language .hex format. It manages 16-bit data from FPGA thanks to an 8 bit parallel port and other 8 standard I/Os and it transfers data packets to the high level SW via the USB integrated port endpoints as well receiving commands from the user. The same I/Os are used to pass the integration time to the FPGA, thus constituting a 16-bit bidirectional port. FPGA Sequencer and DAQ sections can be reset by the user thanks to a dedicated command sent to the microcontroller that acts as asynchronous reset.

It also serially interfaces an Ethernet module to receive commands directly by a LAN network thanks to the TCP/IP protocol. The PIC18F4550 microcontroller is fed by a 20 MHz external clock.

**FPGA FW**

Low-level commands from the microcontroller are decoded by means of a simple 4x16 decoder interfacing the main Finite State Machine implemented inside the VHDL FPGA FW that acts as the brain of the sequencer and data acquisition overall system.

All the controlling finite state machines, decoders, counters, clock dividers, test benches and configuration parameters are organized in separates VHDL files to work in a structured environment managed by the Xilinx ISE Design Suite and ModelSim simulator.

Before synthesizing VHDL SDAQ projects, a test-bench-based simulation is performed by ModelSim to control and assure the optimized operating conditions of the overall design parts (see Fig. 4).

2.4. The high-level graphical user interface

The high-level SW interface (see Fig. 6) was developed under the freely available NOKIA Qt Creator that allows the development of open source software governed by the GNU General Public License (GPL). Qt Creator is a complete integrated development environment (IDE) for creating applications with the Qt application framework. Qt is designed for developing applications and user interfaces once and deploying them across several desktop and mobile operating systems.

It includes:

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- An advanced C++ code editor
- Integrated GUI layout and forms designer
- Project and build management tools
- Integrated, context-sensitive help system
- Visual debugger
- Rapid code navigation tools
- Supports multiple platforms (WinXP, VISTA, Windows 7, Linux, Mac)

The high-level SW interfaces the low-level SW via the USB microcontroller port. We used a simple FW up loader (boot loader) through the USB interface and a graphical interface able to accelerate all the programming tasks.

![Graphical interface](image)

**Figure 6.** The high-level acquisition SW and command interface.

The graphical interface is supported by multiple platforms, like Windows, UNIX and Linux operating systems by means of dedicated libraries and it is used to pass low-level commands to the microcontroller to acquire 16-bit data stored in SRAM memories. Acquired images data are then saved in the FITS format, a standard 16-bit format for astronomical images.
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Furthermore, it is possible to start and stop images acquisition sessions, to start detector-cleaning procedures, to reset the data acquisition system, to set the exposure time and the image array size in pixels units.

3. TESTS AND RESULTS

During the tests, two SDAQ operational modes are available: a "test mode" and a "setup mode". The first mode allows the SDAQ for generating the signals checking the electronics and the general functions of the system, once a specific detector and A/D converting electronics are selected.

When the SDAQ is operated in "setup mode", the parameters for the end-user application are fixed. However, some detector parameters are still configurable also after the controller setup (as exposure time, windowing, pixel binning, array dimensions, pixel rate).

3.1. Experimental set-up and laboratory tests

In the test modality, it is possible to emulate an FPGA internal ADC, to provide 16-bit data to the SDAQ acquisition section. Data values are generated sequentially from 0 to 65535 ADU (16 bit data) and fed by dedicated I/O pins to the input FIFO passing through the 96-pins DIN connector to fully simulate data from an external ADC (see Fig.7). Then, they are acquired and transferred to the microcontroller and to the high level SW interface formatting it in a FITS image. The result is shown in Fig.8.
Figure 7. A SDAQ test set-up for the state logic analyzer.

Every image band showed in Fig. 8 represents 32 shaded rows (65536 grey levels divided by 2048 pixels) necessary to acquire 65536 grey levels stored in the same pixels number. This image, analyzed in details, guarantees the correct acquisition procedure by DAQ. It was tested properly up to an acquisition frequency of 5 MHz, showing always the same structures and characteristics. Moreover, the number sequence representing data from the emulated ADC was checked on the images and on the board by means of a Tektronix TLA 601 state logic analyzer. Checks were performed thanks to some bit test points (see pin strips showed on Fig. 7) located strategically on the board before input FIFO, between FPGA and SRAM memories and between microcontroller and FPGA.
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Figure 8. A 2048 x 2048 pixel image with shading bands representing 16 bit depth grey levels.

All the control signals and phases generated by the sequencer were previously simulated and tested by means of a 1 GHz band-pass LeCroy Oscilloscope, to check for timing characteristics and noise features (e.g. jitter). Phase and control signal counts and sequences were tested via logic state analyzer.

Finally, we performed some images of a test target with the E2V-4240 CCD and the electronic boards developed for the CAOS CCD camera to check the overall SDAQ operation inside the system, obtaining the results showed in Fig.9.

The laboratory tests reported an USB transfer rate to high level interface up to 600 KBytes/s and a total transfer time (including read-out of a 2048 × 2048 pixel CCD test image @ 300 kpixel/s) of 30 s.
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Figure 9. Test target acquired by the SDAQ in the CAOS CCD camera electronics.

4. CONCLUSIONS

In this paper we reported on the development of an innovative sequencer and data acquisition electronics based on an FPGA for a detector timing and signal processing, to be used mainly with CCD sensors, but also with other kind of solid state detectors.

We have described the design of the SDAQ to drive detectors and to acquire their data. It has been developed on a single board, integrating the functionality of a dedicated programmable waveform generator with data acquisition capabilities based on a FPGA and a microcontroller.

A second-generation SDAQ design could be produced, starting by the present, on a radiation hard device implementing redundant logic structures in a structured hardware description language paradigm, to work in a harsh radiation environment like space.
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5. REFERENCES

